A Quick Power Consumption Estimation Method for RTL Compilers

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ABSTRACT
A quick power consumption estimation method for designs generated by RTL compilers which is based on linear and polynomial interpolation is proposed. The method is applied in industrial RTL compilers. The maximum achieved estimation error is 10%.

Keywords
RTL compiler, embedded memories, power consumption, interpolation.

1. INTRODUCTION
Silicon area, performance and testability have been, so far, the major design constraints to be met during the development of digital systems. In recent years, however, things have changed. Power has been given weight comparable to the other design parameters. This is primarily due to the remarkable success of personal computing devices and wireless communication systems, which demand high-speed computations with low power consumption [1]. The rapid increase in design complexity and reduction in design time has resulted in the need for CAD tools that can help make design decisions early in the design process. One of the most important criteria that have to be taken into account while making decisions is power consumption [2]. The accurate power consumption estimation is done with special tools [3], but in case of RTL compilers, when many instances are generated, it is time consuming and inefficient. Hence, to be able to make these decisions early, there is a need for a method to estimate the power consumption from a design description of the circuit at a high level of abstraction. Some techniques have been proposed to estimate the power consumption of a circuit given at a register transfer level description [2]. In [4.5], the authors propose a method to estimate the power consumption given only in a functional view of the design, such as Boolean equation. Practical use of this technique is limited. Paper [6] proposes a high-level metric to estimate the maximum power-up current introduced power gating for leakage reduction. Compared to time consuming logic synthesis followed by gate-level analysis, the high-level estimation has an average error of 21.44% for power-up current. In [7] the authors represent an efficient power estimation method for RTL large design with HDL-aware optimization speedup techniques. Paper [8] proposes a method for high level power estimates based on the total capacitance estimates. Average estimation error was 30.21%.
The [9] we propose a quick area estimation method for RTL compilers and the maximum estimation error was 10%. We would like to explore how the result would be in instance of power consumption. Experimental results showed that the method [9] could be applied in quick estimation of power consumption, which is based on regularity of these descriptions. Hence, in this paper we propose a quick power consumption estimation method for RTL compilers. The maximum achieved estimation error is 10%.

2. METHODOLOGY
RTL compilers are template based [10]. The descriptions generated by RTL compilers are regular. The result of this regularity is that parameterized schemes typically have a modular structure and structural unites of the modules correspond to parameterized features of the scheme. The parameterization of scheme properties is implemented by input parameters of RTL compilers, and allows choosing the required values of properties for the generated design. As a rule, the parameterized properties of scheme refer to the structure and functionality of the scheme and the changes of input parameters bring the corresponding structural and functional changes. The structural and functional changes of parameters bring the quality characteristics changes [11].
In [9] we propose an improved method [11, 12] for quick area estimation of RTL compilers. We mention that there are functional dependencies between quality characteristic of parameterized schemes generated by RTL compilers and input parameters. By finding out analytical representation we can estimate the area of scheme generated by RTL compilers for chosen values of parameters. As the analytical representation of function is unknown, [12] proposes to apply the corresponding approximate function. Power consumption has direct dependency from area and hence is exposed to such a dependency. In this paper we propose a quick power consumption estimation method for RTL compilers which is based on linear and polynomial approximation [13]. Figure 2.1 represents block-scheme of proposed methodology. Method has been applied to in industrial compilers and the maximum achieved estimation error was 10%.

3. STAR MEMORY SYSTEM
Embedded memories are the densest components within a system on a chip (SoC) accounting for up to 90% of chip area. Being designed with aggressive design rules, embedded memories tend to be more prone to manufacturing defects and field reliability problems than any other cores on the chip. Hence, the overall yield of a SoC relies heavily on the memory yield and securing high memory yield is critical to achieving lower silicon cost. New systematic defects are often manifested as yield limiting faults resulting from known factors. To discover the root causes of the yield-limiting factors, adequate diagnosis and failure analysis are needed and accordingly process improvement steps are performed [14].
Today's embedded memories require solutions capable of addressing the yield and reliability needs, such as repair at manufacturing level, diagnosis for process improvement and field repair capabilities.

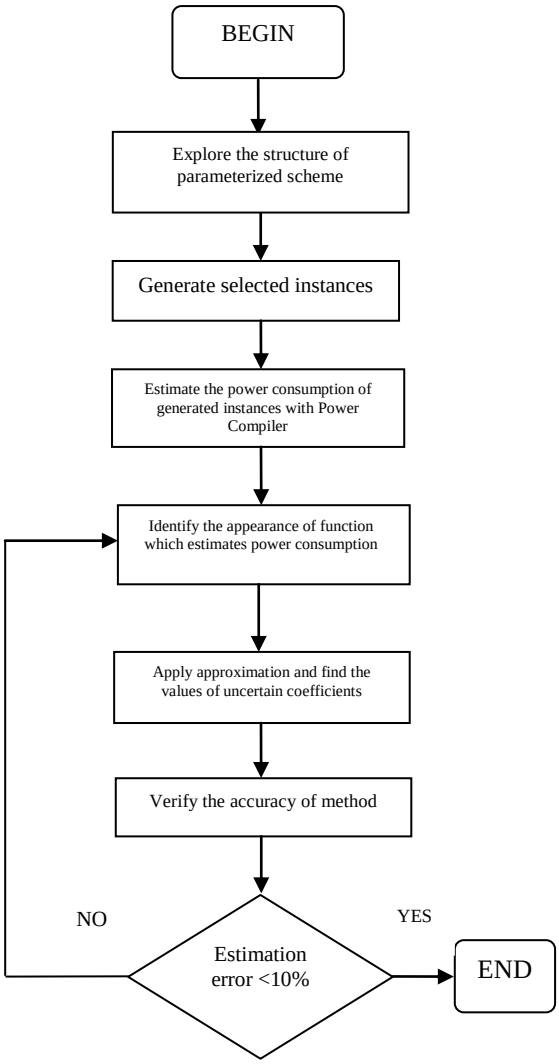

Figure 2.1 Block scheme of proposed method

There are different solutions with built-in self-test (BIST) implementation schemes for solving the mentioned problems [15]-[17]. The Synopsys DesignWare STAR Memory System (SMS) is an end-to-end solution allowing users to generate, automatically integrate, and verify the embedded memory test and repair IP in SoC [14].

Figure 3.1 shows Design Ware STAR memory system infrastructure. It includes Wrappers, Processors, Server and Fuse box.

The STAR Processor performs all the appropriate test and repair coordination of a memory.

The Fuse box may be made of laser fuses to allow Single-Time Repair or may be built of non-volatile to perform Multi-Time Repair.

Wrapper associated with each memory is used in conjunction with the STAR Processor to perform test and repair of the memory as well as allow normal memory functioning in the system [18].

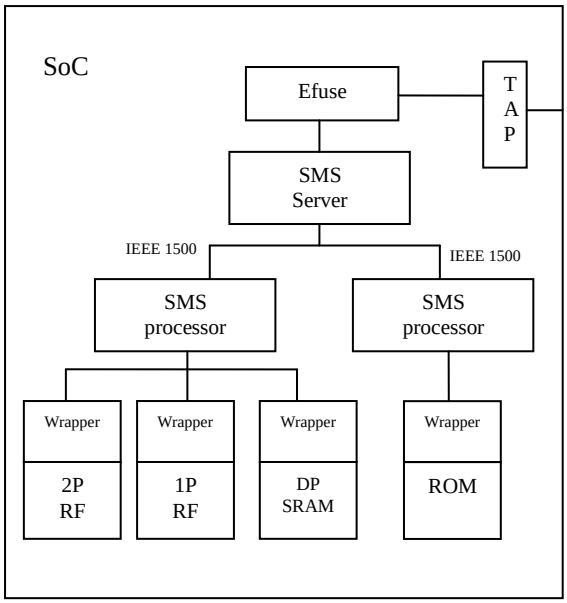

Figure 3.1 Design Ware STAR memory system

4. IMPLEMENTATION DETAILS

The method has been applied to processor and wrapper components of STAR Memory system. Parameters which cause drastic variations in number of gates linearly cause drastic variations in power consumption. Power consumption consists of two main components: static power and dynamic power. The impact of changes of static power is small, hence we explore only the impact of changes of dynamic power.

Experimental results are obtained through Synopsys Power Compiler. A corresponding approximate function have been got after interpolation. The obtained approximate functions are embedded in power consumption estimation script represented in TCL language. The accuracy of method has been verified. The maximum achieved estimation error was 10%.

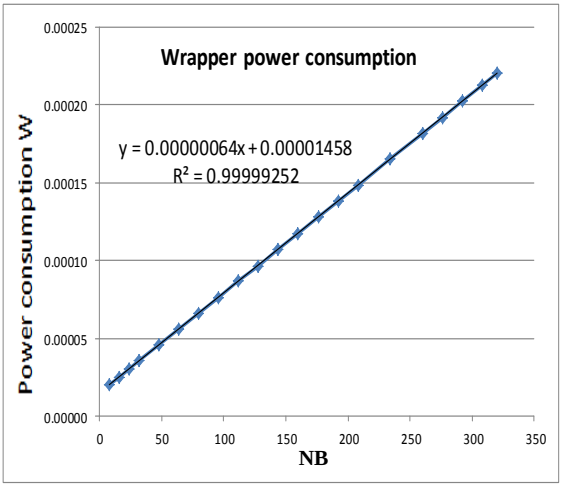

Figure 4.1 Wrapper's power consumption dependency on NB parameter for SRAM type memory

5. CONCLUSIONS

One of the most important quality characteristics of RTL compilers-power consumption has been explored. A quick power consumption estimation method is processed for RTL compilers, which is based on interpolation. The maximum achieved estimation error is 10%.

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