NMOS/PMOS Resistance Calibration Method Using Reference Frequency

Vazgen Melikyan, Abraham Balabanyan, Armen Durgaryan, Artak Hayrapetyan
Synopsys Armenia CJSC
Yerevan, Armenia
e-mail: vazgenm@synopsys.com, abrahamb@synopsys.com, armend@synopsys.com, artakh@synopsys.com

ABSTRACT
A method of NMOS and PMOS transistor resistance variation detection and compensation, using reference clock frequency is presented. The proposed method provides opportunity to measure and compensate MOS device resistance deviation, due to technology process, voltage and temperature variations, separately. Detection of variations is realized using the proposed digital logic block. Efficiency of the suggested method is tested and presented for a high-speed voltage controlled oscillator.

KEYWORDS
Nmos, pmos, resistance variation, calibration, PVT compensation, VCO frequency.

1. INTRODUCTION
With continuous shrinking of CMOS technology sizes and increasing operating frequencies of integrated circuits effect of noise and process, voltage, temperature (PVT) variations [1] on circuit parameters becomes more significant. One of the most important and non-stable parameters of modern technologies is CMOS technology compliant resistor. Usually, such resistors are realized by MOS transistors. Variation of CMOS resistor due to PVT variations can reach about ±50%. Resistance variations of NMOS and PMOS transistors can be different in the same PVT conditions.

Constant resistance values are required in several parts of integrated circuits, such as on-die termination [2]. Signal termination is required to reduce reflections in transmission lines [3]. Excessive transmission line reflections can cause random logic false-triggering. As a result of the mentioned phenomena, the system may fail to function under some operating conditions such as high temperatures or over-voltages.

One of the most effective methods of reducing CMOS resistance variation is the calibration using external high precision resistor (±0.01%). This method provides about ±2% resistance compensation but has some peculiar disadvantages [4]. The main disadvantage is the usage of an external device which creates necessity of having an additional pin on the chip for external resistor. Increasing number of pins on the chip increases production expenses and product cost. If the area of the integrated circuit is not small (more than 1cm^2), then variation of circuit parameters in the far ends of the chip can be different. For more accurate calibration it is suggested to use more than one compensation circuit. For more than one calibration circuits the calibration should be sequential with only one external resistor used at a time. This method increases resistance calibration time in the integrated circuit.

Proposed calibration method provides separate and parallel calibration of NMOS and PMOS transistor resistances without usage of any external additional device. As a reference parameter reference clock frequency (100MHz) of quartz generator, which is used almost in all modern integrated circuits, is used. Proposed method doesn't require additional ports on the chip and the same reference clock frequency can be used by several calibration circuits placed in the far ends of the integrated circuit.

2. PVT VARIATION EFFECTS ON HIGH-SPEED SYSTEMS
As technologies move deeper into sub-micron the manufacturing process non-ideality becomes more pronounced, causing threshold voltage V_{th}, gate thickness and hence oxide capacitance C_{ox} as well as other device key parameter deviations from target (typical) values.

Die temperature constantly changes depending on ambient temperature and IC power dissipation induced heating. Temperature drift manifests itself in transistor threshold voltage and carrier mobility deviations. Supply voltage is also subject to unwanted fluctuations over time.

The mentioned effects usually have adverse effects on high speed system performance. As an example of such system a voltage controlled oscillator (VCO) is considered. VCO is especially unstable to PVT fluctuations [5].

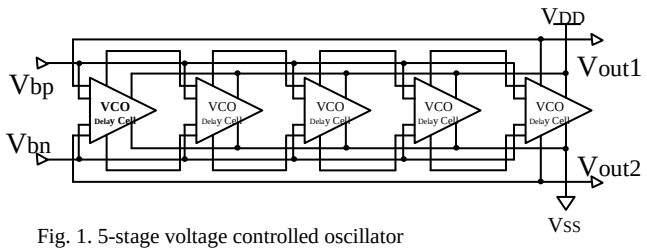

Fig. 1. 5-stage voltage controlled oscillator

For the VCO output frequency the following expression takes place, if biasing circuit is designed correctly:

$$F_{vco} \sim \frac{I_{tail}}{2 * C_n * N * V_{swg}}, \qquad (1)$$

where F_{vco} is the output frequency, I_{tail} is the tail current source current; C_n is the total capacitance at the VCO delay stage output, N is the number of stages and V_{swg} voltage swing in the VCO output. For saturated current tails:

$$I_{tail} \sim k(V_{gs} - V_{th})^2 * (1 + \lambda * V_{ds}), \qquad (2)$$

where:

$$V_{gs} = V_{dd} - V_{bp} = f(V)$$
$$V_{th} = f(\mathrm{P},\mathrm{T}) \quad . \quad (3)$$
$$C_n = f(\mathrm{P})$$

Here V_{gs} is a function of supply voltage, V_{th} is a function of process and temperature and C_n is a function of the process. Compensating these variations separately is not feasible on practice. However, F_{vco} can be effectively compensated if a mechanism for I_{tail} current calibration, depending on F_{vco} variation, exists. This concept is used in this paper.

3. PROPOSED PVT VARIATION DETECTION METHOD

For compensation method to be demonstrated on VCO, circuit is divided into three parts: VCO biasing circuit, ring oscillator and buffering circuit (Fig. 2). V_{ctrl} voltage controls current of VCO biasing circuit which provides V_{bp} and V_{bn} bias voltages for ring oscillator. Buffering circuit contains differential amplifier and buffer for changing oscillator differential outputs to single and signal buffering.

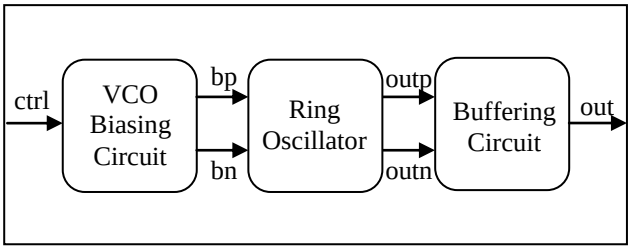

Fig. 2. VCO circuit block-diagram.

PVT detection is based on current variation effect in VCO biasing circuit (Fig. 3).

In VCO biasing circuit, the correctly designed and negative-feedback connected operational amplifier is very stable due to PVT fluctuations. The positive input of operational amplifier in negative feedback circuit gets V_{ctrl} signal which controls VCO output frequency. The second input of operational amplifier duplicates V_{ctrl} voltage and is connected to drain of the resistive NMOS transistor (circled transistor in fig. 3). It operates in triode region and the gate is connected to the highest voltage.

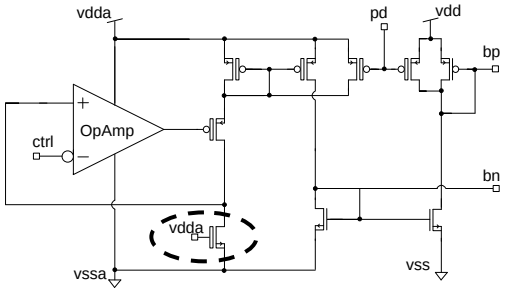

Fig. 3. VCO biasing circuit (NMOS structure).

Drain voltage of the observed transistor is stable and equal to V_{ctrl} so the current flowing through the transistor will be determined by the following equation:

$$I_{NMOS} = \frac{V_{ctrl}}{R_{NMOS}}, \quad (4)$$

where I_{NMOS} is the current flowing through NMOS transistor, V_{ctrl} is the control voltage of VCO and R_{NMOS} is the resistance of triode connected NMOS transistor.

R_{NMOS} is a CMOS resistor based on NMOS transistor which is very unstable to PVT fluctuations. Variations of R_{NMOS} result in variations of I_{NMOS} which flows through VCO biasing circuit current mirror and generates bias voltages responsible for VCO output frequency. So the VCO output frequency variations are only result of NMOS resistance variations

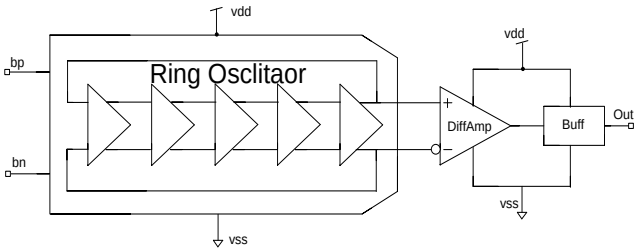

Fig. 4. VCO ring oscillator and buffering circuit.

The inaccuracy of the method is caused by non-ideal VCO biasing circuit which can't replicate I_{NMOS} current to the current mirrors ideally. Inaccuracy of the circuit can be determined by replacing the observed NMOS transistor by an ideal resistor. In ideal case when there are no variations in VCO biasing circuit and ring oscillator, the output frequency will be ideally constant in presence of PVT fluctuations. Simulation results show that the provided method inaccuracy is about 8%.

Presented circuit provides an opportunity to detect NMOS transistor resistance variation due to PVT fluctuations. The proposed method detects and compensates both NMOS and PMOS transistor resistance variations. So for PMOS resistance variation detection another circuit is used. For PMOS structure the only change is VCO biasing circuit. Ring oscillator and buffering block are the same for both NMOS and PMOS structure VCOs. VCO biasing circuit for PMOS resistance variation detection is presented in Fig. 5.

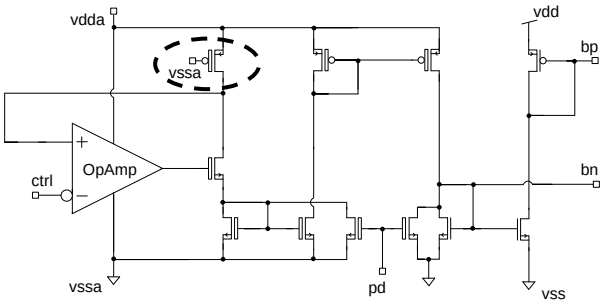

Fig. 5. VCO circuit biasing (PMOS structure).

In this structure as a resistive connected transistor is used circled PMOS transistor. It operates in triode region and the gate is connected to ground. Inaccuracy of PMOS structure biasing circuit is approximately the same as in NMOS one, because their current mirrors are similar and are designed with the same transistor sizes.

4. PROPOSED PVT CALIBRATION METHOD

Proposed method provides an opportunity to realize NMOS and PMOS transistor resistance parallel calibration. As a reference parameter only reference clock frequency of quartz generator is used.

PMOS and NMOS resistance calibration circuit is presented in Fig. 6.

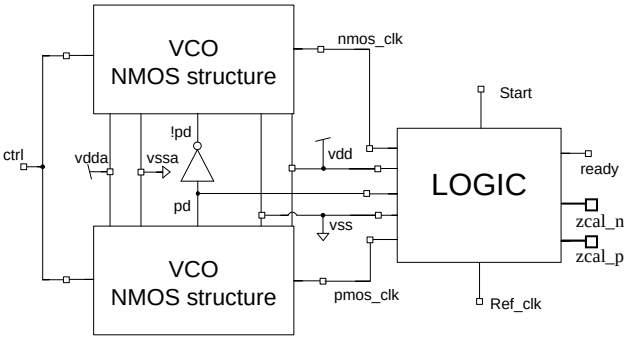

Fig. 6. PMOS and NMOS resistance calibration circuit.

Calibration circuit contains both analog and digital blocks. The analog block contains two VCOs for NMOS and PMOS resistance calibration. The logic block compares VCO output frequency with reference clock frequency. As a result of frequency variation logic block generates N-bit thermometric code which corresponds to the resistance variation. The generated value is the pulse number of the output of VCO circuit during one period of reference clock (usually 100 MHz) due to PVT variations. Knowing the frequency code under typical conditions allows making judgments about frequency deviations. It is assumed that VCO output frequency depends only on detection MOS transistor resistance, so it will have the same deviation.

Logic block is a RTL code which controls the calibration system.

Fig.7. shows simplified timing diagrams for the described compensation mechanism.

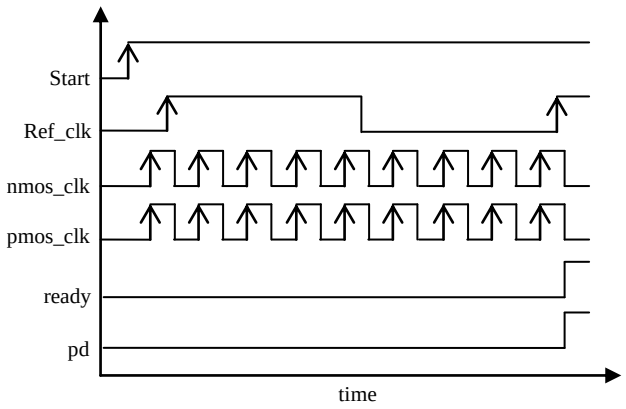

Fig. 7. Logic block simplified timing diagram.

When RTL *Start* input is asserted detection starts with the *Ref_clk* reference clock positive transition (posedge), the system counts NMOS structure and PMOS structure VCO outputs (*nmos_clk* and *pmos_clk*) clock cycles (posedges) until the second posedge transition of the reference clock. With the second posedge transition of *Ref_clk*, logic block writes and saves counted thermometric codes for two VCOs in the registers. After saving calibration codes, operation of counters and decoders is stopped. Thermometric codes are result of decoding the binary code provided by the counters.

At the same moment of calibration *ready* and *pd* output signals of logic block are switched to logic "1". Switched *pd* signal enables power down transistors of NMOS and PMOS structure VCOs. The enabled power down transistors switch off the bias transistors of VCO biasing circuits and current flowing through the circuit becomes zero. Calibration is done at the beginning of chip operation, so power down mode is an important function for minimization power consumption.

Logic block consists of two counters (to count VCO output posedge transitions during *Ref_clk* one period), two decoders (to convert (log_2N)-bit binary counter result to *N*-bit thermometric code), two registers (to save calibration codes) and control block (to control RTL block). RTL block diagram is presented in Fig. 8.

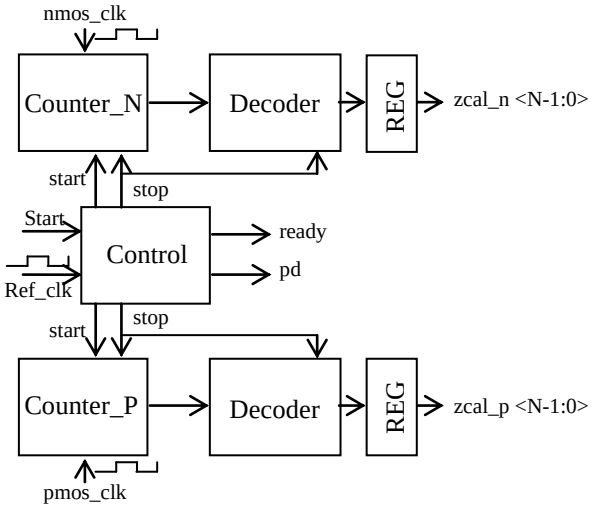

Fig. 8. RTL block diagram.

Calibrated impedance should have *M* times lower value than the detection resistor (4). The actual number *M* is, thus, defined by the target calibration impedance value.

$$M = R_{NMOS/PMOS} / R_{target} \quad (4)$$

Bit numbers of generated impedance calibration code can also vary depending on its application area and target.

In general the proposed calibration method can be used for compensating driver buffer output impedance or input termination impedance in I/O devices. Usually the required value for these resistances is 50 Ohm. Detection MOS transistors in VCO biasing circuits can have any resistance values.

For example, detection PMOS and NMOS transistors have 15k Ohm resistance and it is required to have 50 Ohm resistances for the receiver input pullup and pulldown terminations. Bit number for each calibration code is 32. This means that the target pullup transistor should contain 32 fingers (one PMOS transistor in each finger) and its resistance in typical case should be 50 Ohm. In typical case to have 50 Ohm resistance by fingers, fingers should get middle thermometric code (first 16-bits of *zcal_p* are "0" and last 16-bits are "1"). In this case each PMOS transistor should have 800 Ohm resistance when it operates in triode region. The total resistance of pullup circuit will become the 1/16 part of one PMOS resistance (50 Ohm).

The same principle is realized for pulldown circuit.

Actually, if the bit number of calibration code is N and target resistance is R_{target}, the resistance of NMOS/PMOS transistor in each finger of target circuit should be:

$$R_{finger} = NR_{target} / 2 \quad (5)$$

The larger is bit number N, the more accurate calibration results will be achieved.

5. SIMULATION RESULTS

CMOS resistance variation detection effectiveness is shown in Fig. 9 and Fig. 10. Simulation is performed using Hspice simulator [6] for 39 process corners which include all possible PVT conditions (TT, FF, SS, FS and SF processes with all voltage and temperature values). It is seen from the graphs, that the detection resistance, its current and VCO output frequency variations are very similar for both NMOS and PMOS variation detection structures. Simulation results also show that variation of NMOS and PMOS resistances is not the same: NMOS transistor resistance deviation from typical value (about 15k Ohm) is about 66.7% and for PMOS resistance deviation from the same typical value is about 46.7%. Values of NMOS/PMOS resistances, their currents and VCO output frequencies for three main PVT corners are mentioned in the waveforms.

During calibration, about 700uA current flows through the circuit. The main part of the current flows though VCO biasing circuits which are switched off by power down signal, after calibration is completed.

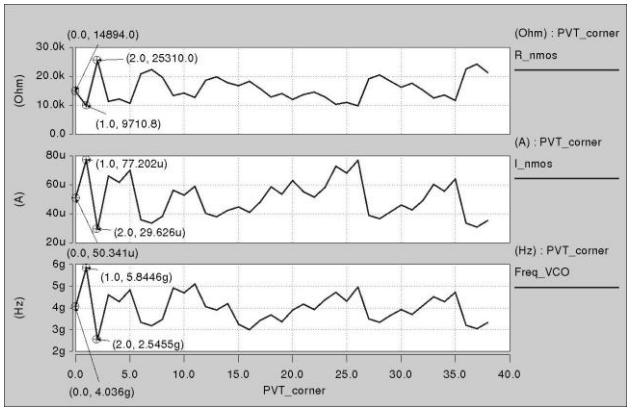

Fig. 9. Detection NMOS resistance calibration effect for all PVT corners.

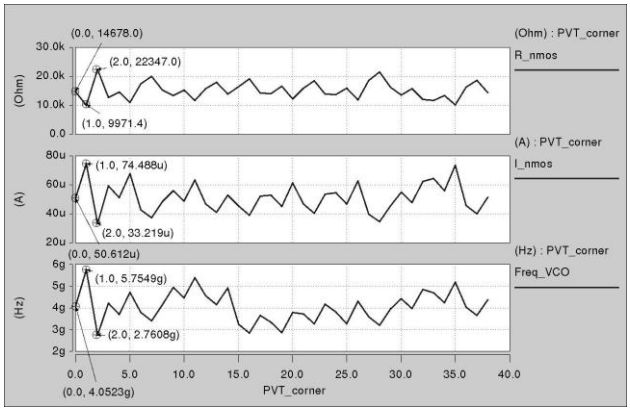

Fig. 10. Detection PMOS resistance calibration effect for all PVT corners.

6. CONCLUSIONS

A calibration method for NMOS/PMOS transistor resistance is proposed and the respective circuit designed. Proposed method allows realizing parallel calibration for NMOS and PMOS which resistance deviations usually are different due to PVT fluctuations.

The considered architecture is based on local VCO frequency comparison to a stable frequency reference. A code obtained from comparison is used for calibration. VCO frequency deviation is a result of its detection bias MOS transistor resistance variation.

Deviation of MOS transistors reaches up to 66.7%. Having circuit output calibration code number higher than 50, allows to decrease PVT variation to 8%. The compensation method inaccuracy is a result of non-ideal operational amplifiers and VCO biasing circuits.

The main advantage of the proposed method is that calibration is realized without usage of any external parameters, such as off-chip high precision resistor. The latter allows to decrease output pin number of the chip and at the same time realizing parallel calibration in the far ends of the chip for more accurate results.

As a reference parameter for calibration 100 MHz reference clock frequency of quartz generator, which always exists almost in all integrated circuits, is used.

Calibration can be realized by using any control V_{ctrl} voltage in a range 0.6-1V. Calibration target resistance value and Z_{cal} generated calibration thermometric code bit number also can be different for a specific system.

Calibration lasts about 0.01u seconds, which is the duration of one reference clock signal period. Upon completion of calibration the circuit is switched to power down mode. During calibration about 700uA current flows through the proposed circuit.

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