ARCHITECTURE OF GAIN-BOOSTED FULLY DIFFERENTIAL OTA WITH RAIL-TO-RAIL INPUTS

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ABSTRACT

A fully differential high-gain and high frequency band width operational transconductance amplifier (OTA) to be used in switched capacitor filters and/or pipeline A/D converters is presented in this paper. The best trade-off is demonstrated between DC gain, speed, and dynamic range performances of input and output signals for this design. The OTA achieves a constant large signal DC gain of > 95 dB over process and temperature variations. It is designed in a 28nm CMOS process and draws a DC power of 6.7 mW from a 1.8-V supply. The settling time to < 0.07% accuracy for the worst case is ~ 7.5 ns. The presented correction technique can be used in the high speed ADCs and in special input/output circuits of several standards such as Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), etc.

Keywords

On trans-conductance Amplifier (OTA), rail-to-rail, gain-boosted, bend width (BW)

1. INTRODUCTION

Typical gain-boosting structures are shown in Fig. 1.Designing analog functional blocks with high gain and large band width under limited supply voltage (0.8-1.8V) becomes more and more difficult. Cascoding technique is the mostly used method to achieve high gain compared to 2-stage OpAmp designs because of its superior frequency response.

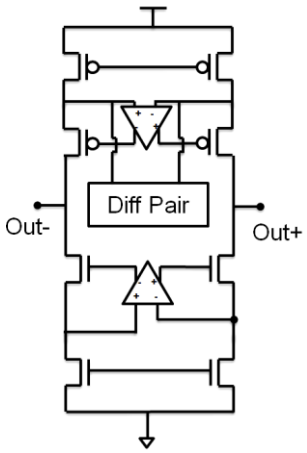


Fig.1. *Gain-Boosting Technique*

The main problem while trying to cascode more transistors is a limited supply voltage. Gain-boosting technique (Fig.1) [1] was introduced to remedy this problem. It allows increasing the DC gain of the operational amplifier without sacrificing the output swing of a regular cascade structure. This can provide high speed and high gain at the same time. Gain-boosted OTA (GB OTA) [2] can have a high gain and can hold in working conditions at high speed systems such as switched capacitor filters (Fig.2) and ADCs. It will cause to heighten the quality performance and exclud input signals inequality. As a result of the mentioned phenomena, the system may fail to function under some operating conditions such as high temperatures or over-voltages.

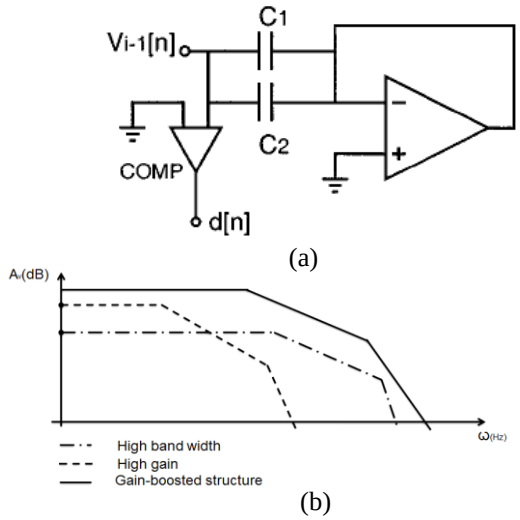


Fig.2. (a) *Gain boosted OTA Using In The i^{th} Stage Of A 1-bit/stage Pipeline ADC*
(b) Bode plot for high band width, high gain and *Gain-Boosting Technique*

It should be noted that it is well known that pole-zero doublets are often associated with gain boosting. Later in simulations results part the result from a small-signal analysis of the gain-boosting technique will be presented. It will become clear that the pole-zero doublets and their consequence (slow settling) (Fig.3.) can be very well suppressed.

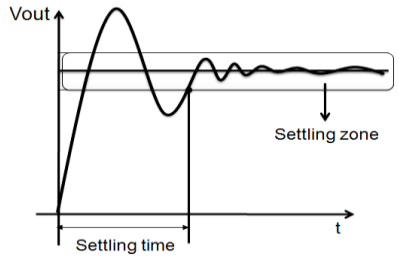


Fig.3. *Settling time calculation*

2. GAIN-BOOSTED OTA CIRCUIT ARCHITECTURE WITH RAIL-TO-RAIL INPUTS

The structure of the proposed GB OTA with Rail-to-Rail inputs is presented in Fig. 4.

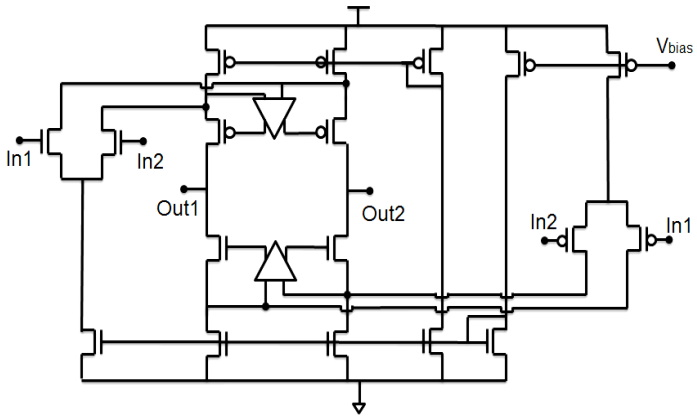


Fig.4. C*ircuit structure GB OTA with Rail-to-Rail inputs*

For increasing input signal range in this architecture it is proposed to use rail-to-rail method. This structure provided high small-signal gain with no frequency band width degradation. Therefore, optimizing the unity-gain bandwidth of the gain booster becomes difficult. A technique used in this paper is to place a small capacitor (usually a MOS cap.) (Fig.5) at the output of the booster to fine-tune.

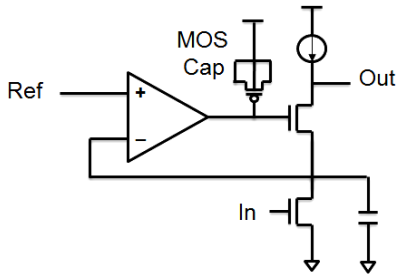


Fig.5. *Using MOS capacitor for booster fine-tunes.*

For minimizing feed forward zero effect capacitive f/b networks provide a feedforward path for input signal to bypass the OTA. Since the f/b is negative, an instant input jump introduces a big spike at the output which is, unfortunately, on the opposite side of the final output voltage. A straightforward calculation yields the following expression for this spike:

$$\Delta V_o = V_o \cdot \beta \cdot \frac{C_f}{C_f + C_L} \quad (1)$$

Since the f/b factor is largely fixed by the closed-loop gain, the only parameter we have control on to minimize the initial spike is the ratio C_L/C_f.

In the ideal OTA, the output current is a linear function of the differential input voltage, calculated as follows:

$$I_{out} = (V_{in+} - V_{in-}) \cdot g_m \quad (2)$$

where Vin+ is the voltage at the non-inverting input, Vin− is the voltage at the inverting input and g_m is the transconductance of the amplifier.

This technique provided high DC gain and as an input signal is acceptable to use high and low common mode voltage levels. This kind of OTA architecture can be used in many high speed structures as a negative feedback system with differential inputs and outputs.

3. OPERATION PRINCIPLE AND AMPLIFYING

Block diagram on Fig 6. has been proposed to amplifying differential signals and having a high frequency bandwidth. As it is known the DC gain value of amplifier is reverse proportional to bandwidth. Thus, it is imperative to have high DC gain in order to avoid unequal distribution when the system is in the negative feedback condition.

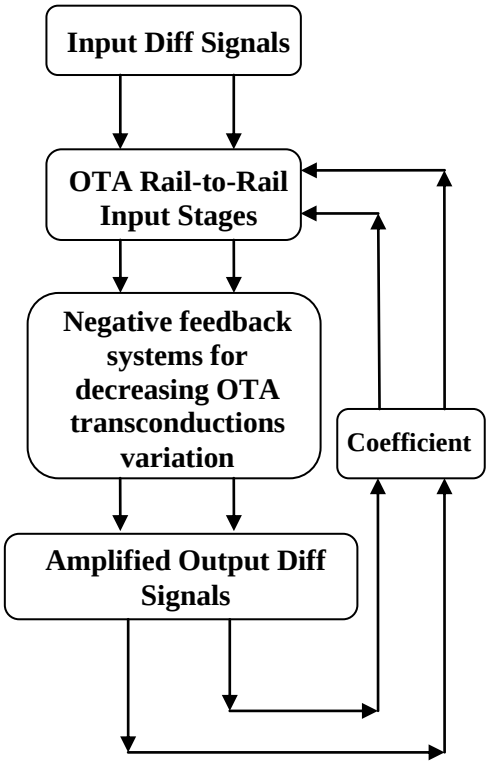


Fig.6. *Block diagram of proposed method with negative feedback*

As it was mentioned above the rail-to-rail inputs are needed for high input signal working range and if possible just with resizing input pairs it can work with full swing input voltage range over PVT.

4. SIMULATION RESULTS

Simulations have been performed to use the circuit level simulator Hspice[4] for 20 PVT corners, including SS (slow-slow), TT (typical-typical), FF (fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations to estimate small-signal gain and the unity-gain BW.

Fig. 8(a) shows OTA alternating current analyses results for TT (55^{O}) typical corner. It is seen that the amplifier's gain is near to 98db and unity-gain BW is about 92MHz.

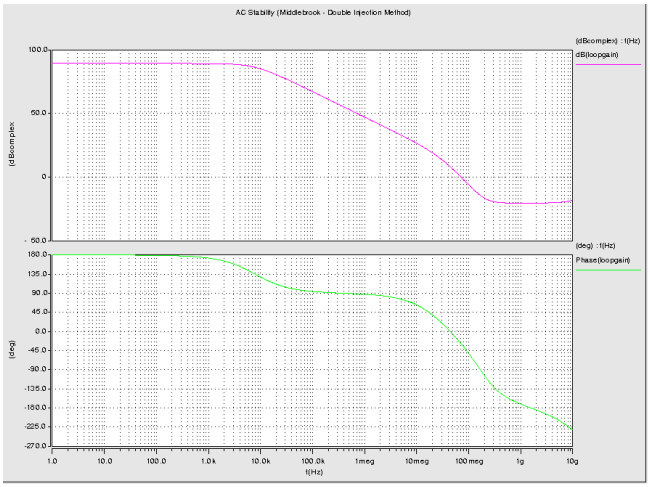
Fig. 8(b) and Fig. 8(c) show simulation results for, respectively, FF (-40^{O}) and SS (125^{O}) main PVT corners.

Taking into consideration that USB3 protocol works with the 5Gb/s data rate signal, which means that Data have 400ps pulse period and 200ps pulse width, we have put internal specification for UGBW, i.e. after duty the cycle can be considered as corrected, when PWE is less than 4ps. In USB3 specification book phase margin min value defined as 45 o.

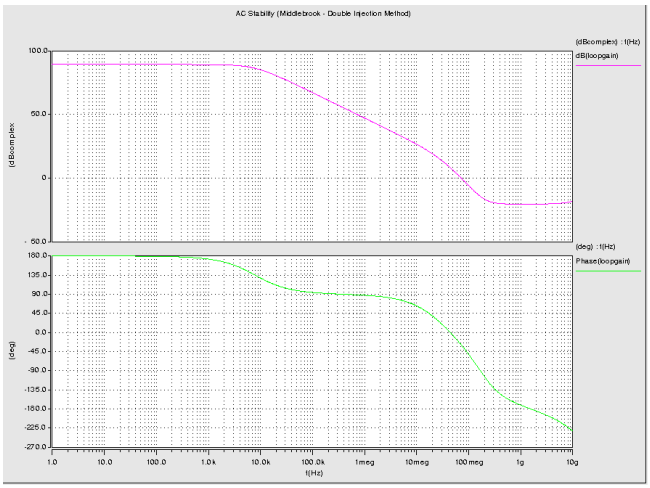
The next important parameter is Settling time (ST), which shows the time when OTA outputs are in settling zone. Table 1 shows the results for 3 main corners.

TABLE I. SIMULATION RESULTS OF THE THREE MAIN CORNERS

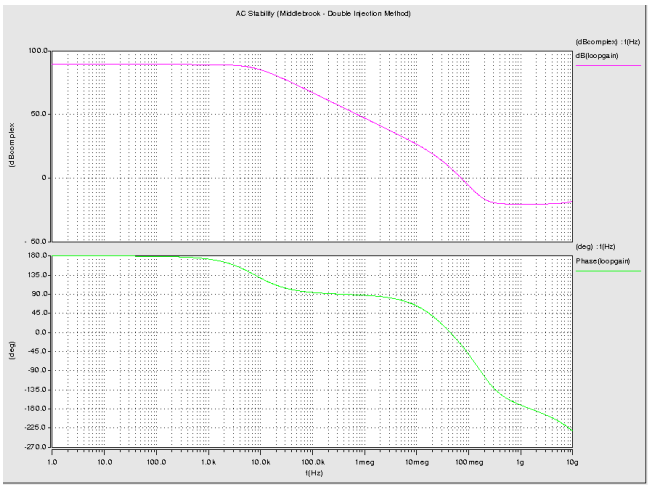
Main Parameters	Bound Corners		
	TT, 25°C	SS, 125°C	FF, -40°C
Diff. Output Voltage Swing (peak-to-peak)	1.8 V		
RMS Output Noise (1 Hz to 100 GHz)	34.2μV	45.4 μV	32.7 μV
Small-Signal A_V *(gain)*	98.4 dB	96.5 dB	101.2 dB
Phase Margin (PM)	82.0 °	85.2 °	83.8 °
Unity-Gain BW	92.0 MHz	85.3 MHz	102.7 MHz
Settling Time	7.1 ns	5.3 ns	3.4 ns
Total Power Consumption	3.05 mW	3.54 mW	3.13 mW



TT (a)



FF (b)



SS (c)

Fig.8. *OTA alternating current analyses results for TT (a), FF (b) and SS (c) corners*

6. CONCLUSIONS

A circuit designed for high speed systems integrated in negative feedback structures. Amplifiers like proposed provided high gain and high working frequency parallelly and can operate in some settling systems as a stable amplifier.

Average Deviation for TT corner is equal to 0.085%, after 7.1 ns of settling time; the BW has the value of 92MHz and PM equal to 82^0 whereas the spec from the USB3 specification book is 45^0.

The approached method can be implemented for input/output protocols such as USB, PCI, etc.

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