Power Optimization Approach of ORCA Processor for 32/28nm Technology Node

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ABSTRACT

This paper presents a method of power optimization implemented on RISC architecture ORCA processor with the help of power gating approach aimed at significant reduction of leakage power consumption. Presented approach results significantly decrease both dynamic and leakage power of ORCA processor when used in combination with multi-voltage power reduction method.

1. INTRODUCTION

ORCA processor is a 32-bit CPU microprocessor core. Microprocessor has two main interfaces: PCI interface and source synchronous DDR interface for SDRAM. The sub-block CLOCK_GEN contains two PLLs (Phase Locked Loop) and a clock multiplier for the functional clocks (Fig.1). These two PLLs cancel the clock tree insertion delay for the PCI I/O interface timing and for the SDRAM input interface timing. The sub-block RESET_BLOCK has a synchronizing reset circuitry for the global, asynchronous prst_n signal. The synchronizing reset circuitry is used during functional mode, but bypassed in test mode. The design has two main interfaces, a PCI interface and an SDRAM with a source synchronous double data rate interface (DDR). The SDRAM bus is capable of addressing PC266 type memory. The DDR data bus is synchronous with both edges of the incoming and outgoing clocks. The processor core consists of a high-speed RISC machine with a power save mode. The BLENDER block is shut down during power save mode and RISC_CORE is slowed down to half its frequency. All asynchronous interfaces between clock domains are isolated with dual-port FIFOs. [3]

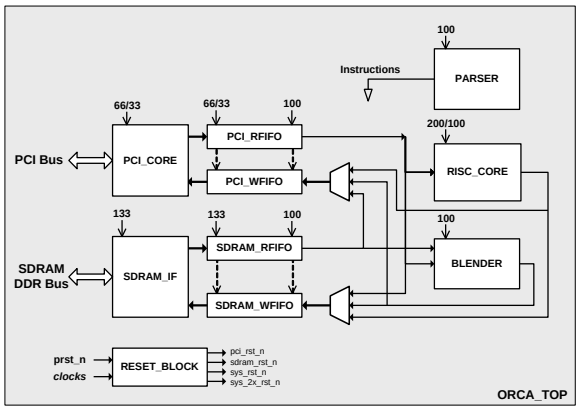

Fig.1. ORCA TOP (functional block diagram)

Control PCI bus is operating at 33 (0) or 66 (1) MHz, Control RISC_CORE operates at 200 (0) or at 100 (1) MHz.

2. PREVIOUS RESEARCH

Previously research of ORCA processor power reduction with multi-voltage method was performed using different voltage supplies for different power domains (RISC core). As a result, power consumption was decreased by about ~15%, compared with standard design, but the area overhead was about ~12%, timing characteristics were globally unchanged (RISC core clock frequency 200MHz). [1]

Frequency	200 MHz
Data required time	20.21 ns
Data arrival time	-20.20 ns
Slack(MET)	0.01 ns
Total Power	75.46 mW (-15%)
Macro/Black Box area	16340.796387 μm^2
Total cell area	661980.75374 μm^2(+15%)
Total area	678321.550135 μm^2(+12%)

Table1. Results of timing/power/area report with multi voltage design method ORCA/RISC core implementation

Deep investigation of ORCA processor structure showed that RISC core consists of more than 1000 registers, and about ~60% of total power is spent on registers [2]. This evidence made it possible to consider power-gating method to be efficient in decreasing power of RISC core. Replacing all registers with retention type will provide power reduction, which at the same time will increase area.

3. THE POWER GATING IMPLEMENTATION

Power gating method is one of the main power reduction methods. For its implementation ISOLATION and RETENTION cells are used in the design. ISOLATION cell usually consists of logic-NAND (with 2 inputs) from the library and two transistors (p-MOS connected to VDD and n-MOS connected to the ground) with the ENABLE signal connected to the gates of transistors (Fig.2).

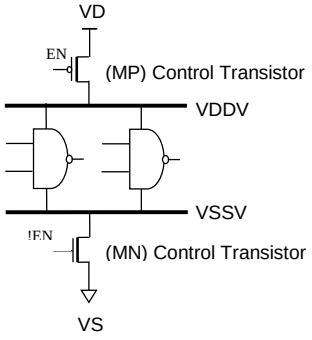

Fig.2. ISOLATION cell structure

ISOLATION cells are placed around the borders of shut-down power domains and effectively keep stable signal at the outputs of the sub-block during inactive mode by the application of ENABLE signal. [5]
During power off (shut-down) mode, there is a necessity to save the state and restore it after wake-up implemented using RETENTION registers (sometimes called SAVE/RESTORE registers) (Fig.3). These have second lower backup power supply (VDDG) which always stays active even when main supply (VDD) is off.

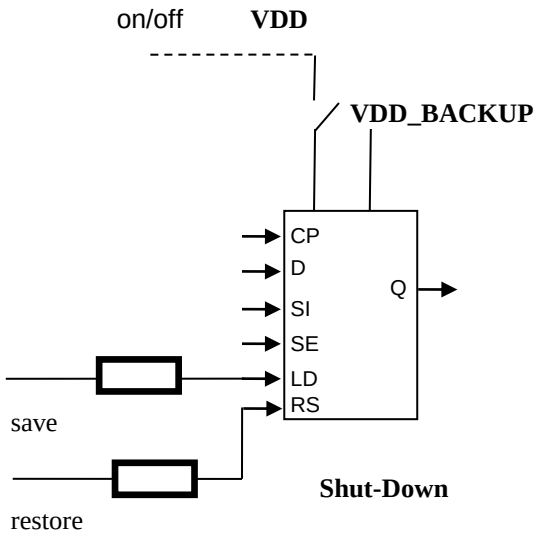

Fig.3. RETENTION register structure

4. DESIGN PROCCES

The design flow of ORCA with power gating method fully fits into standard digital design flow with UPF integration presented in (Fig.4).

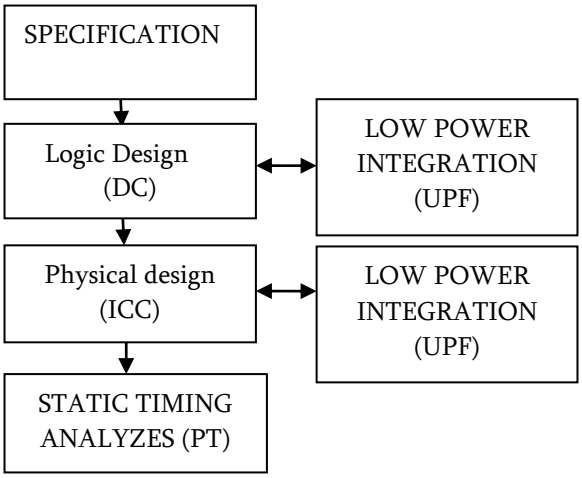

Fig.4. ORCA design steps with power gating method.

During implementation the power gating method was chosen for RISC sub-block as it contains high and low-performance parts. Design specification describes differences between two low power optimization methods (power gating and multi-voltage design [1]). Unified Power Format (UPF) description was developed for power gating implementation in both logic and physical design processes (Fig.5).

```
## CREATE POWER DOMAINS
create_power_domain TOP
create_power_domain RISC   -elements RISC
```

```
## TOPLEVEL CONNECTIONS
# VDD
create_supply_port VDD
create_supply_net  VDD   -domain TOP
connect_supply_net VDD   -ports VDD
create_supply_net  VDD   -domain RISC -reuse
# VSS
create_supply_port VSS
create_supply_net  VSS   -domain TOP
create_supply_net  VSS   -domain RISC -reuse
connect_supply_net VSS   -ports VSS
# VDDG
create_supply_port VDDG
create_supply_net  VDDG   -domain TOP
create_supply_net  VDDG   -domain GPRS -reuse
connect_supply_net VDDG   -ports VDDG
create_supply_net  VDDGS  -domain RISC
-------------------------------------------------------------------------------
## PRIMARY POWER NETS
set_domain_supply_net TOP   -primary_power_net VDD   -
primary_ground_net VSS
set_domain_supply_net RISC  -primary_power_net VDDGS -
primary_ground_net VSS
## RISC SETUP SWITCH
create_power_switch risc_sw \
  -domain RISC \
  -input_supply_port {in VDDG} \
  -output_supply_port {out VDDGS} \
  -control_port {risc_sd PwrCtrl/risc_sd} \
-on_state {state2002 in {risc_sd}}
set_isolation risc_iso_out \
  -domain RISC \
  -isolation_power_net VDD -isolation_ground_net VSS \
  -clamp_value 1 \
  -applies_to outputs
set_isolation_control risc_iso_out \
  -domain RISC \
  -isolation_signal PwrCtrl/risc_iso \
  -isolation_sense low \
  -location parent
# RETAIN
set_retention risc_ret -domain RISC \
  -retention_power_net VDDG -retention_ground_net VSS
set_retention_control risc_ret -domain RISC \
  -save_signal {PwrCtrl/risc_restore low} \
  -restore_signal {PwrCtrl/risc_restore high}

map_retention_cell risc_ret \
               -domain RISC \
               -lib_cells {RDFFNX1 RDFFARX2 }


# ADD PORT STATE INFO
add_port_state VDD   -state {HV  0.95}
add_port_state VDDG  -state {LV  0.7}
add_port_state risc_sw/out -state {LV  0.7}-state {OFF off}
add_port_state VSS  -state {GND  0} ## CREATE PST
create_pst orca_pst -supplies     {VDD VDDG VDDGS }
add_pst_state function1 -pst orca_pst -state {HV  LV   LV  }
add_pst_state sleep     -pst orca_pst -state {HV  LV   OFF   }
```

Fig.5. Unified Power Format (UPF) for power gating

In UPF diagram (Fig. 6) two power domains were defined. Special cells ISOLATION were placed around the boundary of the chosen domain. Standard registers were replaced with RETENTION registers. In the result UPF synthesis used the same design constraints for frequency (for PCI clock at 75 MHz, System RISC clock at 200 MHz, SDRAM clock at 75 MHz) and physical utilization: 30% as multi-voltage design. Values of power, timing and area of power gating and multi-voltage designs are shown in Table 1.

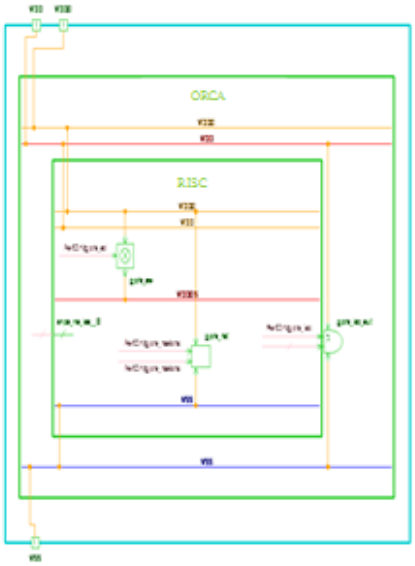

Fig.6. Power gating UPF diagram for ORCA

	Power gating	multi-voltage
Frequency	200 MHz	200 MHz
Data required time	27.48 ns	20.21 ns
Data arrival time	-24.86 ns	-20.20 ns
Slack(MET)	2.62 ns	0.01 ns
Total Power	69.42 mW	75.46 mW ~(- 8%)
Macro/Black Box area	16340.8μm^2	16340.8μm^2
Total cell area	807616.35μm^2(+22%)	661980.75 μm^2
Total area	823956.35 μm^2 ~(+21%)	678321.55 μm^2

Table2. Results of timing/power/area report with power gating design method and multi-voltage design method

Total power of the circuit was reduced by more than 8% compared to multi-voltage design (Table 2), and by more than 23% compared with standard design. However, total area of design increased by ~21% mainly in register cell area (22%). Increased area is due to retention flip-flops being much bigger than standard flops as well as additional isolation cells. 200 MHz frequency is still supported (with increase of 7ns in input to output latency). Differences between power gaiting, multi-voltage design and standard design are presented in Fig. 7 for power and in Fig. 8 for area respectively.

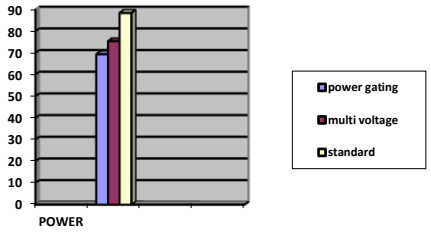

Fig.7. Power consumption for power gating, multi-voltage and standard designs.

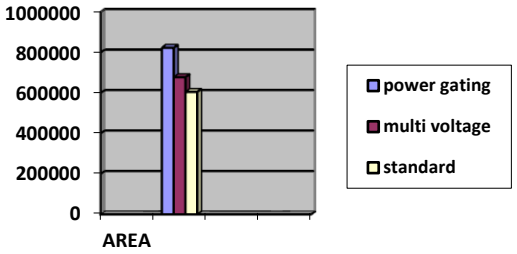

Fig.8. Die area of power gating, multi-voltage and standard designs.

5. CONCLUSION

Power gating design is an efficient method of reduction of ORCA/RISC processors power consumption. Compared with other methods of power optimization [1] (multi-voltage design) power gating is efficient by more than 8% with the same timing specification. Moreover, power gating method is more favorable if area increase can be neglected.

6. ACKNOWLEDGEMENTS

Design was implemented using SAED 32/28nm EDK developed by Synopsys Armenia Educational Department with the help of Synopsys Design Compiler and IC Compiler tools made available by Synopsys Armenia Educational Department [4].

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