Fault Collapsing For Digital Circuits Based On Relations Between Stuck-At Faults^{*}

Tigranuhi Grigoryan, Heghineh Malkhasyan, Gevorg Mushyan, Valery Vardanian

Educational & Research Center of Informational Technologies Yerevan State University Yerevan, Armenia e-mail: vvardani@synopsys.com

ABSTRACT

A way for fault collapsing is proposed for digital circuits based on the relations of fault equivalence and fault dominance. A new notion **of strict structural fault dominance** is proposed for single stuck-at faults on input/output lines of logical gates. Experiments are conducted on combinational circuits of ISCAS'85 and combinational parts of sequential benchmark circuits of ISCAS'89 benchmark circuits. Fault collapsing for most of the circuits is about 60-70%.

Keywords

stuck-at fault, fault collapsing, equivalence, strict dominance

1. INTRODUCTION

Fault collapsing is an approach to alleviate the difficulties connected with the development of test sets for digital circuits. Since it is well-known (see e.g. [1]) that the generation of a test for a single stuck-at fault even for an input line of a combinational circuit is a very difficult problem, then any possible reduction for the number of faults needing development of test sets, is a great benefit. That is why many authors have done research on this topic and some algorithms were proposed for fault collapsing [2]-[4]. As a result, the number of lines needing development of test sets was reduced sometimes up to 50% or even more. Most of the proposed approaches that were classified as structural and functional refer to structural one when the relations of equivalence and dominance were defined between faults on input and output lines of logical gates. An extension of those notions, namely functional equivalence and functional dominance were also defined between any lines in a digital circuit allowing increase the percentage of fault collapsing [2]-[4]. At the same time, functional fault collapsing is a more difficult approach requiring availability of fast commercial programs for test generation of all stuck-at faults on every line in the circuit.

In this paper traditional structural fault collapsing is considered for combinational circuits. Applying a tree-based graph approach to the classical stuck-at faults on gate input/outputs of ISCAS85 and full-scan ISCAS89 benchmark circuits we collapsed the fault sets at average for 60-70%% of faults. The run-time of the algorithm is very fast taking a few seconds at average for a circuit. The results are given in Tables 1 and 2 for ISCAS85 and ISCAS'89 benchmark circuits, respectively. Note that in this work the algorithm works only a few seconds for most of the combinational and sequential circuits from ISCAS'85 and ISCAS'89.

In particular, in this paper the notion of "*strict structural dominance*", an extension of the dominance relation, is introduced.

We showed that although strict dominance applied alone brings to a smaller percentage of fault collapsing than the equivalence relation but, however, when both of the relations are applied then better, than previously known results, can be obtained. Thus, for ISCAS'85 combinational benchmark circuits, most of the results coincide with that of the previously known best results but, however, for a few circuits better results were obtained. For example, for c7552 previously 59.14% and 59.15% of collapsing were obtained, but in our work we obtained 59.41%. For c2670, previously 56.07% and 56.08% of fault collapsing were obtained respectively. In our work we obtained 58.27% of fault collapsing. We applied this approach also for the combinational parts of ISCAS'89 benchmark circuits (fullscan approach). The obtained results were good too. Run time of our program for almost all circuits is a few seconds.

^{*}This work was supported by the State Committee of Science of RA in the frame of scientific project No. 13-B321.

2. MAIN DEFINITIONS

All necessary definitions of fault collapsing and strict dominance can be found in [2]-[4]. In the sequel, we shall use the notation A/c to denote a line A stuck-at-c, $c \in \{0,1\}$. The two concepts widely used in structural fault collapsing are (Structural) *Fault Equivalence* and (Structural) *Fault Dominance*. They were defined in [2] as follows:

Definition 1. (Structural Fault Equivalence) Two single stuck-at faults α and β on an input/output line of a logical gate G in a circuit C are said to be structurally equivalent if and only if $T(C/\alpha) = T(C/\beta)$, where $T(C/\alpha)$ and $T(C/\beta)$ are the complete test-sets for faults α and β respectively.

As to fault collapsing, when faults α and β are equivalent, it is sufficient for removing one of the faults α or β .

Definition 2. (Structural Fault Dominance) A fault α on the output of a logical gate *G* is said to "structurally dominate" another fault β on an input of gate *G* if $T(C/\beta) \leq T(C/\alpha)$, i.e. all test vectors from $T(C/\beta)$ are contained also in test-set $T(C/\alpha)$.

In such a case, all the tests for β can detect α as well. Then it means fault α can be collapsed from the fault list and a shorter test-set T(C/ β) can detect both faults α and β .

Note that two faults will be equivalent if they dominate each other, i.e. $T(C/\beta) \leq T(C/\alpha)$ and

 $T(C/\alpha) \le T(C/\beta)$. Thus, $T(C/\beta) = T(C/\alpha)$, i.e. the test-sets of both faults coincide exactly.

Definition 3. (Structural strict dominance). A fault α on the output of a logical gate *G* is said "to dominate structurally and strictly" another fault β on an input of gate *G* if α structurally dominates fault β but β does not structurally dominate α .

Lemma 1. The output of either of the logical gates AND, OR, NAND and NOR strictly dominates each input of the gate.

Lemma 2. For the logical gate *XOR*, as well as the logical elements *INVERTER* and *BUFFER*, there is no relation of strict dominance between their input and output lines.

3. BRIEF DESCRIPTION OF THE MAIN ALGORITHM

For each gate we construct the so-called "tree of strict dominance". Then for each combinational circuit we construct its "directed graph representation". Then an algorithm is proposed for reduction of the number of faults by using the relations of *strict dominance* and equivalence.

Note that fan-outs of the circuit-graph are also taken into account. The complexity of the algorithm is O(nm) where n is the number of all vertices of the circuit-graph, and m is the maximum number of inputs for all gates in the circuit.

Circuit	Number Of faults	Number of collapsed faults			Reduction (%)	Run
		Equi- valence	Dominance	Equivalence	Equivalence &	(sec.)
				& strict dominance	Strict dominance	
C17	34	-	-	18	52.9	1
C432	864	524	458	469	48.03	1
C499	998	758	730	604	29.26	1
C880	1760	942	763	1015	57.67	3
C1355	2710	1574	1234	1500	55.35	3
C1908	3816	1879	1568	2251	59	4
C2670•	5340	2747	2324	3045	58.99	6
C3540	7080	3428	2882	4304	60.79	8
C5315	10630	5350	4530	6138	57.74	9
C6288	12576	7744	5840	6752	53.69	8
C7552•	15104	7550	6163	8973	59.4	12

 Table 1. Results for combinational circuits from ISCAS85

• For the mentioned circuits the number of faults in our work and in [2]-[4] differ due to the unknown possible

modifications of the circuits in [2]-[4]. There were no details given.

We obtained good results also for the combinational parts of sequential benchmark circuits from ISCAS'89. The results

are shown in Table 2. For some circuits more than 70% collapsing is obtained.

Circuit	Number Of faults	Number of collapsed faults			Reduction (%)	Run
		Equi- valence	Dominance	Equivalence & strict dominance	Equivalence & Strict dominance	time (sec.)
S208	436	217	175	276	63.3	1
S298	596	308	266	336	56.4	1
S344	670	342	277	407	60.7	1
S349	680	350	283	412	60.5	1
S382	764	399	328	459	60.1	1
S386	772	384	295	495	64.1	1
S400	806	426	354	481	59.7	1
S420	916	455	363	582	63.5	1
S444	888	474	388	509	57.3	1
S510	1020	564	441	597	58.5	1
S526	1052	555	474	588	55.9	2
S641	1278	467	421	898	70.3	2
S713	1426	581	519	961	67.4	1
S820	1640	850	702	975	59.5	2
S832	1664	870	718	983	59.1	2
S953	1906	1079	826	1116	58.6	2
S1196	2392	1242	964	1482	61.9	3
S1238	2476	1355	1035	1482	59.9	2
S1423	2846	1515	1214	1720	60.4	3
S1488	2976	1486	1110	1959	65.8	3
S1494	2988	1506	1123	1955	65.4	3
S5378	10590	4603	4034	6726	63.5	8
S9234	18468	6927	5753	13096	70.9	16
S13207	26358	9815	8346	18574	70.5	22
S15850	31694	11725	9564	22631	71.4	25
S35932	71224	39094	30117	41428	58.17	44
S38417	76678	31180	25818	51648	67.36	57
S38584	76864	-	-	49114	63.89	58

Table 2. Results for combinational parts of sequential circuits from ISCAS89

4. ACKNOWLEDGEMENT

The authors would like to thank the following researchers for their support

- Dr. Yervant Zorian, Chief Architect of Synopsys, USA, Foreign Member of the Armenian National Academy of Sciences,
- Prof. Samvel Shoukourian, Research Head of Educational & Research Center of Informational Technologies, Yerevan State University, Full Member of the Armenian National Academy of Sciences,
- Prof. Igor Zaslavsky, Corresponding Member of the Armenian National Academy of Sciences.

REFERENCES

[1] O. H. Ibarra, S. K. Sahni, "Polynomially Complete Fault Detection Problems", *IEEE Transactions on Computers*, pp 242-249, 1975.

[2] V. D. Agrawal, A. V. S. S. Prasad, Madhusudan V. Atre, "It Is Sufficient To Test 25% Of Faults", *Proc.* 7th *IEEE VLSI Design &Test Workshops (VDAT), India*, pp. 368-374, 2003.

[3] A. V. S. S. Prasad, V. D. Agrawal, M. V. Atre, "A New Algorithm for Global Fault Collapsing into Equivalence and Dominance Sets", Prasad et al.: *Proc. International Test Conf.*, pp. 391-397, 2002.

[4] V.C.Vimjam, M.S. Hsiao, "Efficient Fault Collapsing via Generalized Dominance Relations", *VLSI Test Symp.*, pp. 265-271, 2006.