The Estimation of the Surface of a Printed Board

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ABSTRACT

In this work an attempt is made to estimate the surface of the printed board with the help of a mathematical model if the structural parameters of the printed board are known. They resulted from the structural dependence of the printed board on the number of integral schemes (IS) that are placed on the printed board, Rent's coefficient, the average amount of the exits of integral schemes, the smallest width of the metal wire of the printed board and the number of communicative layers of the printed board.

Keywords

integral schemes, layer, printed board, Rent's coefficient, surface.

The choice of the structural parameters of the printed board must be made with such a calculation so that the harmonious correspondence between the structural values was preserved. Besides, the intercellular electrical connections of the functional tie and the wire lengths of those connections also greatly influence the process of the choice of those parameters. Modern great auto programming systems necessarily have prime stages before each stage of preparation and programming, the aim of which is to foresee the essential parameters and characteristics of the scheme from the point of physical realization of the system, especially in the process of dividing the schemes, estimating the opportunities of the solution of the formed problems and the placement of the elements in montage areas [1-9].

Theory

In this work, an attempt is made from the viewpoint of physical feasibility, to determine the functional relation between the PC board surface and the number of conduction layers of the assembly field with the help of a mathematical model, considering that both values are restrictions.

The analysis of the PCB production shows that along with reducing the PCB surface and increasing the number of conduction layers, the amount of spoilage in the production process sharply increases[7].

After preparing the electric schematic diagram, it is very important that the PCB designer approximately estimated the PCB surface and the number of conduction layers, and before completing the installation of the elements and electrical wiring, find out the possibility of its physical feasibility.

As a criterion, the coefficient K of the assembly field occupancy is taken $(0{,}3 \le K \le 0{,}8)$, since it characterizes the density of the wire length of electric connections, and as a connection element – the total length of wires between the electric connections and PCB structural parameters [8]. The aim of modeling is that any part of the function of the object examined is difficult to simplify and present in the form of a model, with the help of which it becomes incomparably easy to observe the basic features that function inside the object.

By saying surface of a printed board we understand the surface that allows to form the wire length of the necessary intercellular electrical ties if the number of integral schemes (chips) are known.

Let's imagine there is an N number of integral schemes (IS-s) with $a \times b$ sizes on the flatboat of the printed board and the amount of IS-s as to the width of the printed board is H, and vertically it is M (Fig. 1). The distance of IS-s in horizontal and vertical directions is respectively equal to $\Delta a, \Delta b$, and here the following rule acts:: $H \times M = N$.

If we have a printed board consisting of a single layer, then by saying the average density of wire lengths of intercellular electrical ties or by saying the amount of layers we would understand the relation of S_{met} surface of wire lengths of metal covered printed board with the S surface of the whole printed board with all its edges. If this technical level allows to create a communication with the least width of $d_{\min}$ on the printed board, then the S surface of the wire lengths will be:

$$S_{met} = d_{\min} \times L \quad , \qquad (1)$$

where L is the sum lengths of wire connections of the intercellular electrical ties.

By the amount of communicative layers we understand S_{met} / S relations:

$$\gamma = S_{met} / S \cdot K \quad , \qquad (2)$$

where S theoretically is the sum surface meant to be covered with metal wires of that layer, K is the fullness coefficient.

The surface of the printed board with the first grade of approximation is found with the following function:

$$S \approx (a + \Delta a)H \cdot (b + \Delta b)M = (a + \Delta a)(b + \Delta b)N \qquad (3)$$

The sum length of the wire connections of intercellular electrical ties in the printed board is equal to:

$$L = L_1 + L_2 \quad , \qquad (4)$$

where L_1 is the length of the wires of electrical ties going to the exits of the printed board from the IS-s distributed on the printed board which we shall call a sum length of external wires.

L_2 is the length of the wires of electrical ties that connect the IS-s distributed on the printed board.

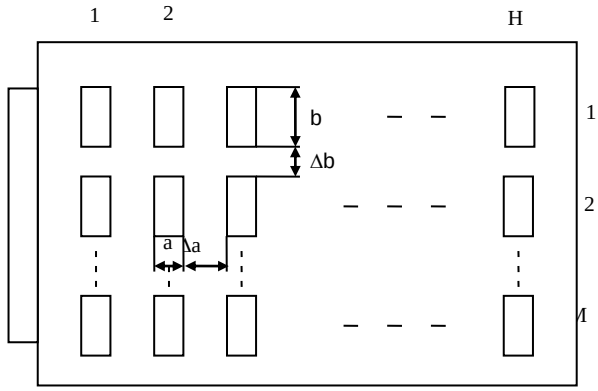

Fig. 1 The overall appearance of the IS-s placed in the printed board

The sum length of the external wires is equal to:

$$L_1 = m(N)\cdot \bar{l}(N), \qquad (5)$$

where $m(N) = m_0 N^p$ is the amount of external ties determined by Rent's law[5].

m_0 - is the average amount of the exits of IS-s, N is the amount of IS-s on the printed board, p is Rent's index $0{,}3 \le p \le 0{,}75$ [5],

$\bar{l}(N) = 0.333\sqrt{(a+\Delta a)(b+\Delta b)N}$ is the average length of external wires[5].

Placing the corresponding $m(N)$ and $\bar{l}(N)$ expressions in the function (5), we shall have:

$$L_1 = 0.333 m_0 \sqrt{(a+\Delta a)(b+\Delta b)}N^{p+0.5} \quad . \qquad (6)$$

Similarly we shall decide the summed length of the external wires of the printed board:

$$L_2 = m_2(N)\bar{l}_2(N), \qquad (7)$$

where $m_2(N) = tm_0\left(N - N^p\right)$ is the amount of internal ties, according to Rent's law[5], t is called the index $(0.5 \le t \le 1)$ of the branches of the chains, $\bar{l_2}(N) = 0.666\sqrt{(a+\Delta a)(b+\Delta b)N}$ is the average length of internal wires[5].

Using the corresponding $m_2(N)$ and $\bar{l}_2(N)$ expressions, we shall have the sum length of the internal wires:

$$L_2 = 0.666 m_0 t\sqrt{(a+\Delta a)(b+\Delta b)}\left(N^{\frac{3}{2}} - N^{P+0.5}\right). \qquad (8)$$

Placing the corresponding L_1 and L_2 expressions in function (4), we shall have the sum lengths of the wires in the printed board:

$$L = 0.333 m_0 \sqrt{(a+\Delta a)(b+\Delta b)}\times \times\left(2tN^{\frac{3}{2}} + (1-2t)N^{P+0.5}\right) \quad . \qquad (9)$$

The surface of the printed board in case of one-sided exits will be:

$$S_{one-sided} = \frac{S_{met}}{\gamma\cdot K} = \frac{1}{3\gamma\cdot K} m_0 d_{\min} \times \times\sqrt{(a+\Delta a)(b+\Delta b)}\left[2tN^{\frac{2}{3}} + (1-2t)N^{P+0.5}\right]. \qquad (10)$$

If there are no external exits:

$$S = \frac{S_{\text{met}}}{\gamma\cdot K} = \frac{2}{3\gamma\cdot K} m_0 . d_{\min} \times \times\sqrt{(a+\Delta a)(b+\Delta b)}\left[2tN^{\frac{3}{2}} - N^{P+0.5}\right]. \qquad (11)$$

If we install the formula (3) in (11), we will obtain the dependence of the conduction layer number on the quantity of the elements.

$$\gamma = \frac{2m_0 d_{\min}}{3K\sqrt{(a+\Delta a)(b+\Delta b)}}\left[2tN^{0.5} - N^{P-0.5}\right]. \qquad (12)$$

Using the function (10) of the determination of S, we can observe the functional dependence of the printed board upon the N amount of IS-s and γ amount of printed layers.

For example: in case of $t = 0.5$, $m_0 = 10$, $d_{\min} = 0.2cm$, $(a+\Delta a) = 6cm$, $(b+\Delta b) = 4cm$, K=0.6, $p = 0.5$ values the dependence of S of the printed board upon the N amount of IS-s is shown in Fig.2, and upon amount of the layers is shown in Fig.3.

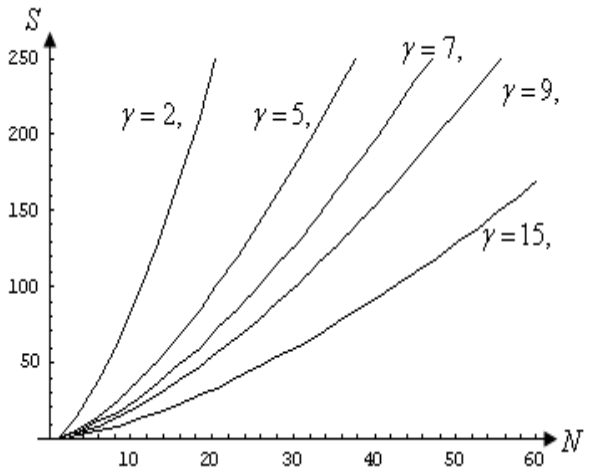

Fig. 2. The dependence of the surface of the printed board upon the N amount of IS-s

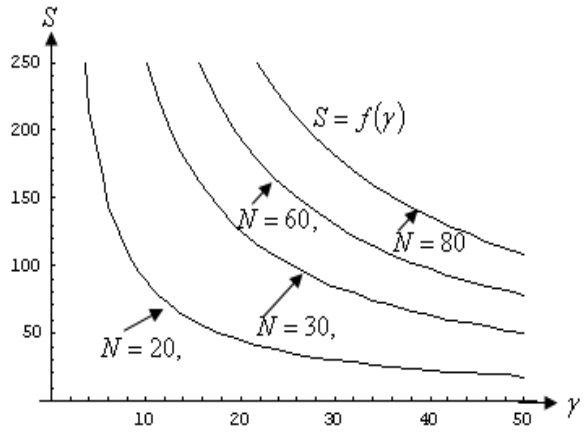

Fig. 3. The dependence of S of the printed board upon γ amount of layers

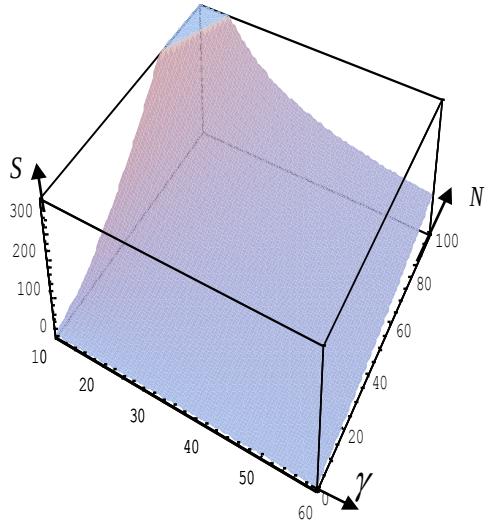

Fig. 4. The dependence of the surface of the printed board upon γ amount of layers and the N amount of IS-s

CONCLUSION

Thus, we got the functional dependence of surface of the printed board upon the N amount of IS-s, as well as upon Rent's index p, the $a \times b$ sizes of chip and the $\Delta a, \Delta b$ amounts of their distribution, the m_o amount of chip average exits, the γ amount of communicative layers and the smallest width of $d_{\min}$ of communicative layers.

As it is seen in Fig. 2, the S of the printed board grows with the growth of the grade of integration, and fig.3 shows that the S of the printed board becomes smaller with the growth of the communicative layers. Thus, the equations (10) and (11) that we have got enables us to find the S of the printed board in the earliest stage of designing from the point of physical realization.

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