ISO 26262 Compliant Memory BIST Architecture

David Sargsyan

Yerevan State University
Yerevan, Armenia
e-mail: davvad93@gmail.com

ABSTRACT

The modern automotive industry has entered an era where tendencies are towards the increased automation and connectivity. The proportion of electronics-controlled systems is steadily growing in vehicles. In parallel the safety and reliability requirements to automobiles are becoming more stringent due to the increased number of accidents with fatalities on the roads. The problem is complicated by the fact that automotive has started to use cutting-edge technologies irrespective of their maturity level. This paper describes the use of BIST implementations for self-test of memories in an automotive SOC, to support testing in mission mode. Case study at the end of the paper demonstrates a practical built-in self-test architecture implementation providing efficient solutions for both production and in-field testing.

Keywords

automotive, safety, ASIL, built-in self-test, in-field test.

1. INTRODUCTION

The automotive is one of the fastest growing sectors in semiconductor industry at the moment. The reasons of such tremendous growth in automotive market are the increasing consumer demands in safety, reliability and security enhanced applications. The tendency for greater safety and better driving experience is forcing automakers to continually integrate more and more Electronic Control Units (ECU) like Advanced Driver Assistance Systems (ADAS) and In-Vehicle Infotainment (IVI) into their vehicles. Some of the examples of such systems are adaptive cruise control, parking assistance, automotive emergency braking, lane change assistance, and so forth. Automotive electronic systems have traditionally utilized the well-established technology node process for the benefit of higher yield, reliability and low cost. However, considering the growing demands automakers had to adopt the solutions with increased computing power and communication performance. As the International Technology Roadmap for Semiconductors (ITRS) diagram in Fig. 1 shows in the past only the technologies with enough maturity level were allowed to be used in automotive electronics and the technology maturity period was counted to be about five years in average. Nevertheless, especially during the last ten years, with the growing consumer market pressure, this margin has significantly decreased reaching up to two years. Such trends pose additional challenges for automotive application designers to meet the requirements for higher performance and power efficiency along with the native demands for safety, robustness, reliability and time-to-market. As a result, the modern automotive industry faces the following major challenges:

- Functional safety and reliability
- High quality testing
- Data management and connectivity
- Security and privacy
- Design-specific aspects

One of the most important aspects to take into consideration while designing applications for automotive is functional safety and reliability requirement, thus they must have high test quality.

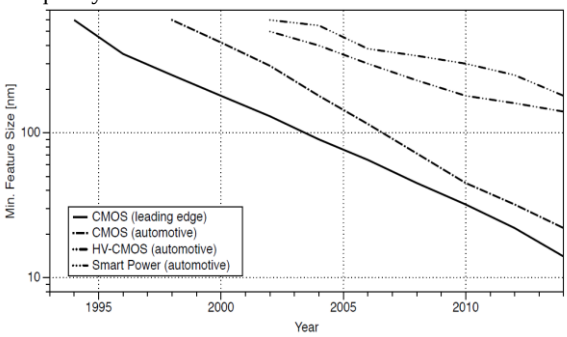

Fig. 1. International Technology Roadmap for Semiconductors (ITRS), Update 2012, [1]

Especially this concerns the embedded memories spanning most of the System-on-Chip (SoC) space and being the main contributors to achieving high yield and low defective parts per million (DPPM) rate. With the growth of ADAS and IVI systems in vehicles, the demands for higher safety and reliability are growing at the same rate. The main objective of safety and reliability is tolerating the risk of physical injury or of damage to the health of people. The increased attention to safety and reliability aspects in automotive motivated the emergence of dedicated ISO 26262 Standard. It defines the requirements for achieving acceptable level of risk for electrical and/or electronic systems intended to be used in production automobiles. Based on the adherence to these requirements a final product can be qualified with one of available four automotive safety integrity levels (ASIL) A-D. ASIL refers to an abstract classification of inherent safety risk in an automotive system or elements of such a system. ASIL classifications are used within ISO 26262 to express the level of risk reduction required to prevent a specific hazard, with ASIL D representing the highest and ASIL A the lowest. The ASIL assessed for a given hazard is then assigned to the safety goal set to address that hazard and is then inherited by the safety requirements derived from that goal. ASIL is determined based on a combination of the probability of exposure, the possible controllability by a driver, and the possible outcome's severity if a critical event occurs. Below the related work concerning various testing aspects in automotive is presented.

In the next section of this paper testing modes for automotive are presented. Section 3 is devoted to discussion of ISO 26262 standard for automotive safety and the product qualification flow. Section 4 describes memory BIST architecture in production and mission modes respectively. Section 5 concludes the paper.

2. TESTING MODES FOR AUTOMOTIVE

The need for high level of safety and reliability in automotive industry leads to necessity of having robust test and repair solution not only at production but also in the field. The traditional test solutions used in the manufacturing are not applicable for the field testing, so there are several specialized solutions proposed with this regard including Power-On Self-Test (POST), Periodic testing for permanent faults detection, Error Correcting Codes (ECC) dealing with the transient faults detection and correction and also aging detection mechanisms. These techniques are detailed further in this section.

A. Production mode testing

One of the conceptual requirements for automotive is the supreme product quality, which can be assured with high yield and low DPPM criteria for the produced chips. During the manufacturing process, it is achieved with the help of efficient test and repair algorithms. For this purpose, at the design stage most commonly Design-for-Testability and built-in self-test (BIST) blocks are incorporated into the chip which are later being used for test, debug and diagnosis operations. There are already efficient test algorithms developed which provide full coverage for each class of faults but they have different complexities and therefore different runtime requirements. In the case of automotive, runtime and performance requirements are usually sacrificed to the benefit of higher fault coverage meaning that advanced test algorithms can be used.

B. Power-on mode testing

Enabling the test also in the field is a specific requirement for functional safety-oriented applications. In contrast to manufacturing, in the field the requirements to test are more stringent due to number of area, power and time-related constraints. Therefore, several alternative solutions are proposed aimed to fulfill them. One such type of in-field test is POST. This test starts whenever a car is turned on. In contrast to manufacturing test, where test algorithm can be programmed, in POST test algorithms are hardcoded and cannot be modified afterwards. The main goal of POST is to quickly test whether all devices are properly connected and accurately functioning before the car is turned on and report if any issue is found. The other functionality of POST is related to memory repair. During the manufacturing, the repair signature is stored in eFuse array, and that information must be sent to memory at power-on. Since the POST time is short, there is a strong requirement to transfer that information faster.

C. Mission mode testing

Another type of in-field test which is used in mission mode is Periodic test. Periodic test ensures that the device has not become unsafe since the POST was performed. The Periodic self-test starts at least once per safety interval, which is defined by safety-critical devices as a period of time during which failure can occur. The first difference of POST and Periodic test is that during the Periodic test there is no need to have repair option. The main goal of Periodic test is to check if there is an issue in a device, and inform driver about it. The second difference is that they have different test flows. For example, during the memory test, POST flow is the same as the manufacturing test, but Periodic test flow is different since the content of the memory should not be erased. Currently the trends are towards having a POST architecture in automotive which will also support Periodic test.

The other type of testing used in mission mode is error-correction code (ECC). The techniques discussed above targeted the testing of hard faults, nevertheless, in order to adhere safety and reliability requirements there is a need to address also soft errors occurring in mission mode. The main cause of such errors are alpha particles emitting in integrated circuits and cosmic rays coming from the outer space as discovered in recent studies [3]-[4]. Soft errors, compared to hard errors, have transient nature and do not cause a permanent damage.

With regard to reliability concerns in automotive, it is also important to consider circuit aging phenomenon and its consequences. The main causes of aging are NBTI (Negative Bias Temperature Instability) and HCI (Hot Carrier Injection) effects, but recently also PBTI (Positive Bias Temperature Instability) effect importance has increased. With this regard, several mechanisms are proposed in the literature for monitoring aging effects, and ultimately tolerating or mitigating them [2], [8] and [5]. The second phenomenon which causes faults in semiconductor is electromigration (EM). Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. EM reduces via/contact dimension and increases resistance, which causes resistive bridges and resistive opens, and may cause word-line timing fault in memory array [7].

3. ISO 26262 STANDARD AND ASIL-X CERTIFICATION PROCESS

Safety is one of the key issues of future automobile development. With the trend of increasing technological complexity, software content and mechatronic implementation, there are increasing risks from systematic failures and random hardware failures. ISO 26262 is a Functional Safety standard, titled "Road vehicles – Functional safety" and it defines functional safety for automotive equipment applicable throughout the lifecycle of all automotive electronic and electrical safety-related (E/E) systems. ISO 26262 includes guidance to avoid these risks by providing appropriate requirements and processes. Automotive Safety Integrity Level refers to an abstract classification of inherent safety risk in an automotive system or elements of such a system. ASIL classifications are used within ISO 26262 to express the level of risk reduction required to prevent a specific hazard, with ASIL D representing the highest and ASIL A the lowest. The ASIL assessed for a given hazard is then assigned to the safety goal set to address that hazard and is then inherited by the safety requirements derived from that goal. ASIL is determined based on a combination of the probability of exposure, the possible controllability by a driver, and the possible outcome's severity if a critical event occurs.

Fig. 2 shows the ASIL-X certification process for a given product. It consists of the following major steps:

1. Product is provided to Certifier
   - Assume that the product that is being certified is an ECC scheme.
2. Certifier identifies Safety Goal Violations (SGVs) of the product
   - Safety Goal (SG) is a safety requirement assigned to a product with the purpose of reducing the risk of one or more hazardous events to a tolerable level
   - Safety Goal Violation (SGV) is a violation of a safety goal due to a fault in the product

- Assume that Certifier identified the following SGV for ECC scheme: **"ECC functionality incorrect"**.

3. Certifier identifies Failure Modes (FMs) of the product
   - Assume that Certifier identified the following FM for ECC scheme: **"Incorrect data bit on ECC Encoder"** as SPF (Single Point Fault);
   - Faults that lead directly to the violation of a safety goal are called Single Point Faults (SPFs);
   - MPFs (Multiple Point Faults) are combination of multiple independent faults leading directly to the violation of a safety goal.
4. Certifier calculates Diagnostics Coverage (DC) for each FM and SGV
   - In this step Certifier identifies the impact of each FM on each SGV and the corresponding Diagnostic Coverage (DC) of the product able to detect that impact;
   - In case of ECC, Certifier would identify that FM **"Incorrect data bit on ECC Encoder"** has direct impact on SGV **"ECC functionality incorrect"**;
   - Assume that ECC scheme has an in-field fault injection mechanism using which it will be possible to detect FM **"Incorrect data bit on ECC Encoder"** with 99.99% Diagnostic Coverage (DC).
5. Certifier calculates ASIL-X level based on DC numbers
   - Based on obtained DC number and using well-known table (see Table 1) from ISO 26262 standard, Certifier calculated that ECC scheme satisfies ASIL-D requirements.
6. Certifier calculates FIT rate of the product
   - Using well-known formulae, Certifier calculated FIT rate of ECC scheme to be equal to 1.7FIT.
7. Certifier prepares FMEDA report
   - FMEDA report contains all the information obtained during the certification process including SGVs, FMs, DCs, ASIL and FIT numbers.
8. Certifier provides final ASIL-X level certificate
   - In case of ECC scheme, Certifier would provide ASIL-D level certificate.

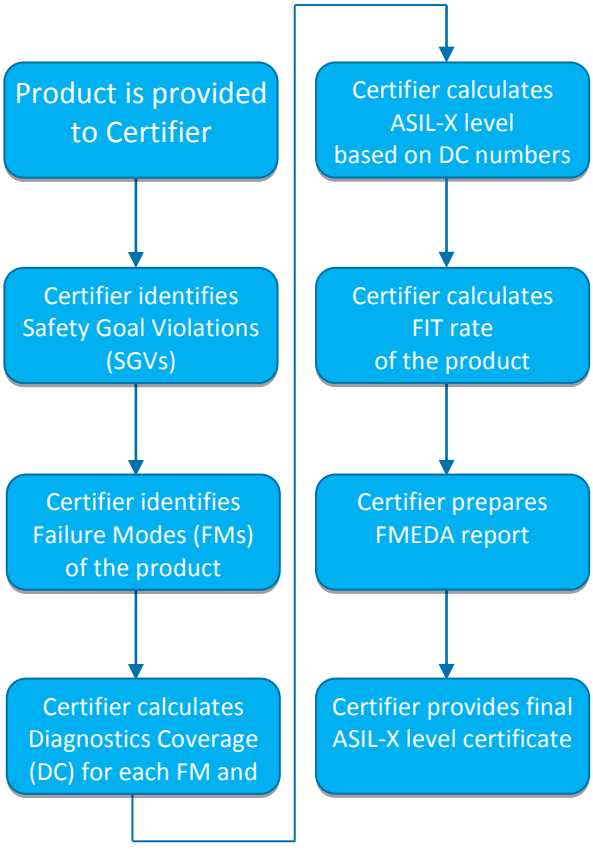

Fig. 2. ISO 26262 certification process

Table 1. ASIL and FIT requirements

ASIL	SPF	MPF	FIT Rate
ASIL B	≥ 90 %	≥ 60 %	100 (recommended)
ASIL C	≥ 97 %	≥ 80 %	100 (required)
ASIL D	≥ 99 %	≥ 90 %	10 (required)

4. ISO 26262 COMPLIANT MEMORY BIST ARCHITECTURE

The case study in this section demonstrates a built-in self-test and repair solution for automotive. Synopsys STAR Memory System (SMS) [6] is an industry leading solution for embedded memories test and repair for more than 10 years and provides a comprehensive set of test, repair and diagnostics features. SMS is based on a flexible BIST implementation with advanced capabilities for addressing methods, background data patterns, test operations programmability and test algorithms construction. Recently SMS solution was enhanced with a set of advanced features to expand its facilities into the field of automotive. These enhancements allow to support high quality test and repair not only at production but also during the power-on and mission modes. Due to loose requirements to test time in production mode, the default recommendation in SMS is to use complete set of available test algorithms in order to achieve high yield and low DPPM rate. During the power-on mode the goal is checking if memory is properly functioning in the limited period of time. For this purpose, SMS provides the efficient test algorithm that quickly tests memory for the most probable faults such as stuck-at, stuck-open, transition and read destructive faults and runs the repair flow if necessary. The architecture of MBIST in production mode is shown in Fig. 3. A typical MBIST includes test access port (TAP), address generator (AG), data generator (DG), test algorithm register (TAR) and comparator.

- JTAG test access port, which can send commands either serial or parallel
- Controller takes commands ("Start test", "Select algorithms group", etc.) from TAP and gives to TAR.
- TAR holds information about March elements (addressing direction, addressing type, operation code and pattern).
- Background pattern generator (BPG) generates test data based on pattern type.
- AG selects which memory cells must be tested, based on addressing direction and addressing type.
- Comparator checks memory output against the expected correct data pattern.

Fig. 4 shows MBIST architecture in mission mode. In this

case the test process organization is a little bit different. The aim here is ensuring the memory is not affected by faults without corrupting its content. The solution provided by SMS is based on the concept of on-line Periodic test which was discussed in Section 2. With this regard, SMS was enhanced with:

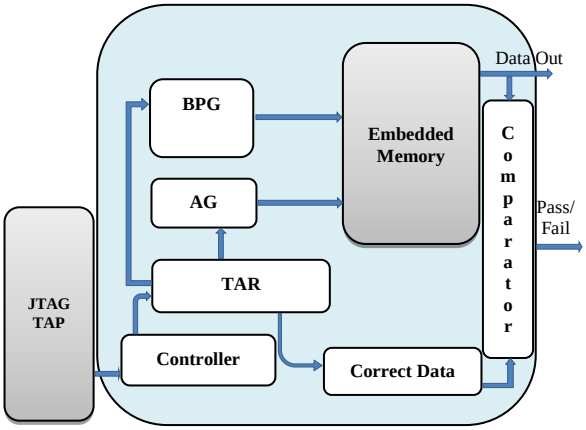

Fig. 3. Memory BIST architecture in production mode

- Reserve register, where the content of the memory under the test is temporarily stored;
- The capability to test the specific memory range;
- New test operations for storing and restoring the memory content.
- New test access port which will allow to do system test during mission mode.

The size of the reserve register and the address range are programmable parameters and can be adjusted during the production based on application specifications. The whole test procedure is controlled by the smart scheduling algorithm which continually monitors which memories are busy and which can be tested at each specific point of time. Due to the critical time constraint, the complex test algorithms cannot be used during the in-field test, however running the tests periodically compensates this to some extent and minimizes the risk of fault escapes.

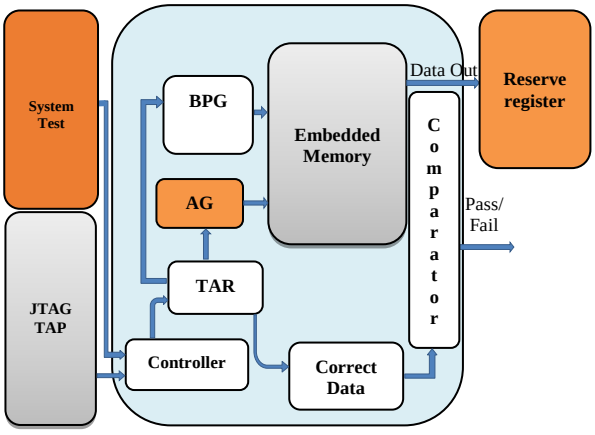

Fig. 4. Memory BIST architecture in mission mode

Another feature of SMS in mission is multibit error detection and correction code which is designed to protect not only the data paths of memories but also address decoders from transient faults. Finally, one more important feature of SMS in mission mode is the constant self-monitoring capability of BIST since it is also prone to aging and other negative effects as the other parts of the system. At the end, it is important to mention that SMS test solution was certified with ASIL-D certificate as ISO 26262-compliant and automotive-ready product.

5. CONCLUSION

Automotive is one of the fastest growing consumer markets for semiconductor industry. The high standards of quality, safety, reliability and related aspects in automotive result in new challenges for leveraging already community-proven solutions. This especially refers to testing aspects since the high-quality testing requirements throughout the whole product life-cycle are far more rigid for automotive. In this paper at first the quick introduction to automotive industry is presented with the comprehensive overview on its various aspects including safety, reliability and testability.
Afterwards, the built-in test solution demands and concepts are explained for various operating modes of vehicles including production, power-on and mission. Finally, the details on efficient test solution for automotive testing implemented in the context of STAR Memory System are provided in Section 4.

REFERENCES

[1] International Technology Roadmap for Semiconductors, Update 2012. [Online]. Available: http://www.itrs2.net.

[2] J. C. Vázquez et al., “Built-in aging monitoring for safety-critical applications”, IEEE European Test Symposium (ETS), 2009, pp. 9-14.

[3] Tezzaron Semiconductor, “Soft Errors in Electronic Memory – A White Paper”, http://www.tezzaron.com, Jan. 2004.

[4] R. C. Baumann, “Radiation-induced soft errors in advanced semiconductor technologies”, IEEE Transactions on Device and Materials Reliability, Vol. 5, No. 3, pp. 305-316, Sep. 2005.

[5] C. Guardiani et al., “An I-IP based approach for the monitoring of NBTI effects in SoCs”, IEEE International On-Line Testing Symposium (IOLTS), 2009, pp. 15-20.

[6] K. Darbinyan, G. Harutyunyan, S. Shoukourian, V. Vardanian, Y. Zorian, “A Robust Solution for Embedded Memory Test and Repair”, IEEE Asian Test Symposium (ATS), 2011, pp. 461-462.

[7] Woongrae Kim, Soonyoung Cha, Linda Milor, “Memory BIST for On-Chip Monitoring of Resistive-Open Defects due to Electromigration and Stress-Induced Voiding in an SRAM Array”, Georgia Institute of Technology, 30332, Atlanta, GA, USA, E-mail: wrkim@gatech.edu.

[8] R. Vattikonda, W. Wang, Y. Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," Design Automation Conference, 2006, pp. 1047-1052.